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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application for:

Trung Nguyen, et al.

Serial No.: 09/767,364

Filing Date: 01/22/2001

For: HIGH SPEED ENVELOPE DETECTOR AND METHOD

Examiner: Kerveros, James C.

Group Art Unit: 2133

APPEAL BRIEF

COMMISSIONER FOR PATENTS
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Sir:

This is an Appeal from the final rejection of claims 1-11 in the above-referenced application. In accordance with 37 C.F.R. § 41.37, this Brief is filed along with the accompanying Appendices and the required fee. Please charge any additional fees or credit any overpayment to Deposit Account No. 501128.

I. REAL PARTY IN INTEREST

The real party in interest to this Appeal is Cadence Design Systems, Inc., a Delaware Corporation, having its principal place of business in San Jose, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellants, the Appellants' legal representative, or assignees thereof.

III. STATUS OF CLAIMS

Claims 1-11 are pending in the present application. The Examiner has rejected claims 1-11. Appellants hereby appeal the rejection of claims 1-11.

IV. STATUS OF AMENDMENTS

One amendment to the application was submitted after final rejection. This amendment has been acted upon by the Examiner and was denied entry for the purpose of the appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. Independent Claims

A. Claim 1

Claim 1 recites an envelope detector for determining whether the level of a differential input signal DPIN – DNIN is above a reference voltage VREF. *See* Figure 1. The envelope detector includes a voltage-to-current converter stage that converts the differential voltage input signal to a differential current IDP – IDN and the reference voltage to a reference current IREF. *See, e.g.,* Figure 3; and page 3, line 25 thru page 4, line 20. The envelope detector also includes a comparator stage that determines whether the differential current level is greater than the reference current. *See, e.g.,* Figure 4 and page 4, line 22 thru page 6 line 5. The envelope detector further includes an output detector that provides an output signal indicative of when the level of the differential current is greater than the reference current. *See, e.g.,* Figure 5 and page 6, line 14 thru page 7, line 4.

B. Claim 4

Claim 4 is the method claim analogue of the circuit recited in claim 1. Claim 4 recites a method of determining whether the level of a differential input signal DPIN – DNIN is above a reference voltage. The method converts the differential input signal to a differential current IDP – IDN. *See, e.g.,* Figure 3; page 3, lines 25-28; and page 4 lines 5-16. The method also converts the reference voltage to a reference current IREF. *See, e.g.,* page 3, lines 28-31; Figure 3; and page 4, lines 5-16. The method then compares the currents to determine whether | IDP – IDN| is greater than IREF. *See, e.g.,* Figure 4 and page 4, line 22 thru page 6 line 5. The method finally provides an indication of a valid differential signal when |IDP – IDN| is greater than IREF. *See, e.g.,* Figure 5 and page 6, line 14 thru page 7, line 4.

C. Claim 6

Claim 6 recites an envelope detector for determining whether the level of a differential input signal DPIN – DNIN is above a reference voltage VREF. The differential input signal is cyclical with DPIN and DNIN each being greater than the other during alternate cycles and crossing over during a switching interval between the cycles. *See, e.g.,* Figure 1. The envelope detector includes a voltage-to-current converter stage that converts the differential voltage input signal to a differential current IDP – IDN and the reference voltage to a reference current IREF. *See, e.g.,* Figure 3; and page 3, line 25 thru page 4, line 20.

The envelope detector also includes a comparator stage that compares the currents and provides an output signal indicative of a valid differential signal when |IDP – IDN| is greater than IREF. *See, e.g.,* Figure 4 and page 4, line 22 thru page 6 line 5. The envelope detector further includes an output detector that maintains the output signal during the switching interval following a

cycle in which the level of the differential current is greater than the reference current. *See, e.g.,* Figure 5; and page 6, line 14 thru page 7, line 4.

D. Claim 9

Claim 9 is the method claim analogue of the circuit recited in claim 6. Claim 9 recites a method for determining whether the level of a differential input signal DPIN – DNIN is above a reference voltage VREF. *See, e.g.,* Figure 1. The differential input signal is cyclical with each input being greater than the other during alternate cycles and crossing over during a switching interval between the cycles. *See, e.g.,* Figure 1; and lines 4-11. The method converts the differential input signal to a differential current IDP – IDN (*See, e.g.,* Figure 3; page 3, lines 25-28; and page 4 lines 5-16) and converts the reference voltage to a reference current IREF. *See, e.g.,* page 3, lines 28-31; *See, e.g.,* Figure 3; and page 4, lines 5-16. The method then compares the currents to determine whether |IDP – IDN| is greater than IREF. *See, e.g.,* Figure 4 and page 4, line 22 thru page 6 line 5. The method also provides an output signal that indicates a valid differential signal when |IDP – IDN| is greater than IREF. *See, e.g.,* Figure 5 and page 6, line 14 thru page 7, line 4. The method maintains the output signal during the switching interval following a cycle in which |IDP – IDN| is greater than IREF. *See, e.g.,* Figure 6.

2. Dependent Claims

A. Claim 8

Claim 8 is dependent on claims 6 and 7. Claim 8 recites all limitations of claim 6. Also, claim 8 on its own or through its dependence on claim 7 recites the following additional limitations. The comparator stage in the envelope detector includes a comparator for comparing IDP – IDN with

IREF (*see* Figure 2; and page 4 lines 18-19) and a comparator for comparing IDN – IDP with IREF. IREF (*see* Figure 2; and page 4 lines 19-20). Also, the means for providing the output signal includes an OR circuit coupled to the comparators for providing the output signal when IDP – IDN > IREF or IDN – IDP > IREF. *See* Figure 5; and page 6 lines 12-23. Furthermore, in order to maintain the output signal, the output detector includes a Schmitt trigger that is responsive to the output signal from the OR circuit. *See, e.g.,* Figure 5; and page 6, line 24 thru page 7 line 4.

B. Claim 11

Claim 11 is dependent on claim 9. Claim 11 recites the additional limitation of passing the output signal through a Schmitt trigger. The trigger levels of the Schmitt trigger is set further apart than a change in the output signal during the switching interval. *See, e.g.,* Figure 5; and page 6, line 24 thru page 7 line 4.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether the subject claims 1-7 and 9-10 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent. 4,890,066 to Straver et al. ("Straver") in view of U.S. Patent 6,556,535 to Kobayashi ("Kobayashi").

II. Whether the subject matter of claims 8 and 11 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent. 4,890,066 to Straver et al. in view of U.S. Patent 6,556,535 to Kobayashi and further in view of U.S. Patent 4,809,554 to Shade et al. ("Shade").

VII. ARGUMENT

The Examiner erred in rejecting the claimed invention by misapplying standards under 35

U.S.C. §103(a).

A. The Subject Claims 1-7 and 9-10 are Patentable under 35 U.S.C. 103(a) over Straver in View of Kobayashi

In rejecting the subject claims 1-7 and 9-10 under 35 U.S.C. 103 (a) the Examiner stated the following:

> Regarding Claims 1-7, 9 and 10, Straver substantially discloses an envelope detector for generating a full-wave rectified signal in response to a differential input signal (Is-Ic) Fig. 2, comprising:
>
> Means differential amplifier (A), for converting the differential input signal (Is-Ic), into a pair of current signals (i1-i2) and the reference voltage (+Vb) to a reference current (I1-I2), as shown in Fig. 2.
>
> Straver does not disclose comparing means to determine if the differential input signal (Is-Ic) is greater than the reference current (I1-I2), and indicating means for indicating the differential signal is valid when it is greater than the reference. Kobayashi, in an analogous art, discloses (Fig. 1) an envelope detector 9 including a comparator 12, which compares the output signal of the amplifier 10 and the reference erasing power value and delivers the result of comparison to the current amplifier 13, which sets an amount of laser diode 14. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a comparator 12 and indicating means diode 14, as taught by Kobayashi, in the envelope detector of Straver, for the purpose of determining the differential input signal, since the reference of the comparator can be adjusted accordingly to respond to variations of the differential input signal, thus resulting in a more reliable envelope detection.

(Office Action mailed October 19, 2004, pages 2-3)

It is the burden of the Examiner to establish a prima facie case of obviousness when rejecting claims under 35 U.S.C. §103. In re Piasecki, 754 F.2D 1468, 223 USPQ 758 (Fed. Cir. 1985). To establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In this case, Appellants respectfully submit that the Examiner has not established the prima facie case of obviousness, as the suggested combination of the references does not teach or suggest all the claim limitations. Specifically, Appellants respectfully submit that (1) the cited combination of references does not disclose, teach, or suggest an envelope detector with a differential input signal, (2) the cited combination of references does not disclose teach, or suggest an envelope detector that converts a reference voltage to a reference current, and (3) the cited combination of references does not disclose, teach, or suggest an envelope detector that compares a differential current with a reference current. These three points are further described in subsections 1 to 3 below.

Moreover, the mere fact that references can be combined or modified does not render the resultant combination obvious, unless the prior art also suggests the desirability of the combination. In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000). It is improper to use the inventor's disclosure as a road map for selecting and combining prior art disclosures. Grain Processing Corp. v. American Maize-Products Corp., 840 F.2d 902, 907 (Fed. Cir. 1988). Absent such a showing in the prior art, the Examiner has impermissibly used "hindsight" by using the Appellants' teaching as a blueprint to hunt through the prior art for the claimed elements and combine them as claimed. In re Zuko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997).

As further described in subsection 4 below, the Examiner's rejection has relied on impermissible piecemeal, hindsight combination of features from different references. This hindsight, piecemeal reconstruction is specifically problematic as the Examiner has not identified any suggestions or motivations in the art for establishing this combination.

1. Cited References Do Not Disclose, Teach, or Suggest an Envelope Detector with a Differential Input Signal. The Examiner Erred in

Identifying Is – Ic as Differential Inputs to the Envelope Detector in Straver

The differential input signal DPIN – DNIN of claims 1-7 and 9-10 is not disclosed by any of the cited references. DPIN and DNIN are two external inputs that are cyclical switching signals which alternate in level during successive cycles and cross over during a switching interval. *See*, e.g., Figure 1; Page 1, lines 4-6; and claims 1, 4, 6, and 9. In Straver, the only external input to the envelope detector is Is. *See* Straver Figure 2. In the Office Action mailed on 10/19/2004, the Examiner identified Is – Ic as a differential input to the envelope detector. The envelope detector in Straver, however, does not have differential inputs. It only has one input which is Is. The Ic signal is an internal negative feedback that is used to reduce an unwanted D.C. level in the output. *See*, Straver Figure 2; and column 4, lines 26-29. This is in contrast with the present invention in which two external inputs DPIN and DNIN are applied to the envelope detector and their values are subsequently converted to currents. *See*, e.g., DPIN and DNIN in Figure 2; and A and AN in Figure 3.

Similarly, Kobayashi does not specify an envelope detector with differential inputs. *See* Figure 1, item 9. Moreover, Kobayashi's invention is not about envelope detectors and the envelope detector in Kobayashi is shown only as a block diagram with only one input. *See* Figure 1; and column 3 lines 32-35.Therefore, neither Straver, nor Kobayashi disclose, teach, or suggest an envelope detector with differential inputs.

2. Cited References Do Not Disclose, Teach, or Suggest an Envelope Detector That Converts a Reference Voltage to a Reference Current. The Examiner Erred in Identifying +Vb as a Reference Voltage in the Envelope Detector in Straver

The reference voltage VREF of the present invention is not disclosed by Straver. In the Office Action mailed on 10/19/2004, the Examiner has referred to +Vb in Straver as a reference voltage. *See* Figure 2. Straver, however, identifies this voltage as a power supply voltage. *See* Straver Column 3, lines 28-33 and lines 46-47. The reference voltage VREF in the present invention is, however, different than the power supply voltage. The reference voltage is an external input to the envelope detector that is converted to a reference current which in turn is used for comparison with the differential current levels.

Also, in regard to converting the reference voltage to a reference current, in the Office Action, the Examiner has specified that in Straver, +Vb (the alleged reference voltage identified by the Examiner) is converted to a reference current (I1 – I2). Straver, however, specifies the two currents I1 and I2 as mutually equal collector current sources (*See* Column 3, lines 30-31), i.e., the difference between I1 and I2 is ideally zero as oppose to be differential currents whose values are normally different and their difference is being used as a reference value.

Furthermore, Kobayashi does not specify converting a reference voltage to a reference current either. *See* Figure 1. Therefore, none of the references disclose, teach, or suggest converting a reference voltage to a reference current as is done in the present invention.

3. Cited References Do Not Disclose, Teach, or Suggest an Envelope Detector That Compares a Differential Current with a Reference Current

In the Office Action mailed on 10/19/2004, the Examiner stated that Straver does not disclose comparing means to determine whether the differential input signal (Is-Ic) is greater than the reference current (I1-I2). The Examiner was correct in stating that Straver does not have such a comparing means. For the reasons indicated in Sections B.1 and B2 above, however, the Examiner erred in identifying Is-Ic as differential inputs and I1-I2 as reference currents. Moreover, the Examiner erred in indicating that Kobayashi specifies such a comparator.

Specifically, the envelope detector in Kobayashi receives only one input and generates only one output. This output is then amplified and compared to a reference voltage representing an erasing power value. *See*, Figure 1; and Column 3 lines 32-42. There is, however, no indication of a differential current value being compared to a reference current. Therefore, neither cited references, disclose, teach, or suggest comparing a differential current with a reference current as specified in claims 1, 4, 6, and 9.

4. The Examiner Rejected the Claims by Relying on Impermissible Piecemeal, Hindsight Combination of References

Appellants respectfully submit that the Examiner's rejection is relying on an improper hindsight and piecemeal reconstruction for rejecting claims 1-7 and 9-10. In the Office Action mailed on 10/19/2004, the Examiner correctly specified that Straver does not disclose comparing means to determine if the differential input signal is greater than the reference current and indicating means for indicating the differential signal is valid when it is greater than the reference. The Examiner, however, cited Kobayashi for disclosing an envelope detector that includes a comparator for

comparing the output signal of an amplifier and the reference "erasing power value" and delivering the result of the comparison to the current amplifier, which sets an amount of laser diode.

However, Appellants respectfully submit that the Examiner, in making this rejection, did not identify any suggestion or motivation in the art for combining the two references. Without the identification of a suggestion or motivation to combine the cited references, the examiner has not met his prima facie case of obviousness.

Moreover, Appellants respectfully submit that Kobayashi teaches away from including a comparator and means of generating an output indicative of a valid differential input in the envelope detector. In the present invention, the claims recite an envelope detector that includes a comparator. In Kobayashi, the comparator is a component external to the envelope detector. In fact, this comparator is separated from the envelope detector by another component. *See* Kobayashi Figure 1, items 9 and 12. Furthermore, in Kobayashi the diode identified by the Examiner is used to combine a recording power with an erasing power rather that to indicate a valid differential input. *See* Kobayashi Figure 1, item 14.

The cited references, therefore, do not suggest the desirability of the combination and the Examiner has impermissibly used hindsight by using the Appellants' own claims as a template for combining features from different references for the claimed elements. The only motivation the Examiner has offered is that the teachings are analogous art. Even if the two cited references are from an analogous art, being from analogous art by itself does not satisfy the burden of establishing a suggestion or motivation to combine two references. Therefore, the Examiner has not met the burden of establishing prima facie case of why it makes sense to combine these references. Moreover, as

mentioned above, the references teach away from including a comparator and means of indicating a valid input inside an envelope detector. Therefore, one of ordinary skill will not be motivated to combine the references for the claimed elements.

B. The Subject Claims 8 and 11 are Patentable under 35 U.S.C. 103(a) over Straver in View of Kobayashi and in Further View of Shade

In rejecting the subject claims 8 and 11 under 35 U.S.C. 103 (a) the Examiner stated the following:

> Regarding Claims 8 and 11, the combined reference of Straver and Kobayashi fails to disclôse a Schmitt trigger responsive to the output signal, wherein the output signal is passed through the Schmitt trigger having trigger levels set further apart than a change in the output signal during the switching interval. However, Shade, in an analogous art, discloses (Fig. 1) an envelope detector 29 including a full-wave rectifier 26 coupled to a low-pass filter 36 with the output connected to the input of Schmitt trigger 38. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the combined device of Straver and Kobayashi, by connecting the output of its filter to a Schmitt trigger, as taught by Shade, for the purpose of detecting the output level corresponding to the differential input signal, since the Schmitt trigger acts as background average device by smoothing the measured points, thus resulting in the reduction of unwanted background noise and erratic measurements.

(Office Action mailed October 19, 2004, pages 3-4)

It is the burden of the Examiner to establish a prima facie case of obviousness when rejecting claims under 35 U.S.C. §103. In re Piasecki, 754 F.2D 1468, 223 USPQ 758 (Fed. Cir. 1985). To establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In this case, Appellants respectfully submit that the Examiner has not established the prima facie case of obviousness, as the suggested combination of the references does not teach or suggest

all the claim limitations. Specifically, as discussed in more detail in subsection 1 below, Appellants respectfully submit that the cited combination of references does not disclose, teach, or suggest the use of a Schmitt trigger inside an envelope detector for the purpose of smoothing out the effects of signal glitches in the output voltage.

Moreover, there must be some suggestion or motivation to modify the reference or to combine reference teachings. In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000).The mere fact that references can be combined or modified does not render the resultant combination obvious, unless the prior art also suggests the desirability of the combination. In re Kotzab, supra. It is improper to use the inventor's disclosure as a road map for selecting and combining prior art disclosures. Grain Processing Corp. v. American Maize-Products Corp., 840 F.2d 902, 907 (Fed. Cir.1988). Absent such a showing in the prior art, the Examiner has impermissibly used "hindsight" by using the Appellants' teaching as a blueprint to hunt through the prior art for the claimed elements and combine them as claimed. In re Zuko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997).

As further described in subsection 2 below, the Examiner's rejection has relied on impermissible piecemeal, hindsight combination of features from different references. This hindsight, piecemeal reconstruction is specifically problematic as the Examiner has not identified any suggestions or motivations in the art for establishing this combination.

1. Claims 8 is Indirectly Dependent on Claim 6 and Claim 11 is Directly Dependent on Claim 9 Which are Argued to be Patentable in Section A Above. Furthermore, the Examiner Erred in Comparing the Role of the Schmitt Trigger in Shade with the Schmitt Trigger in claims 8 and 11.

Claims 8 is indirectly dependent on claim 6, and claim 11 is directly dependent on claim 9. For the reasons discussed above for claims 6 and 11 in Section A, claims 8 and 11 are also patentable over the cited references. Furthermore, the Schmitt trigger of claims 8 and 11 is responsive to the output of the comparator (OR) and is set further apart than a change in the output signal during the switching interval. *See, e.g.,* Figure 6, item 77; and page 8, lines 1-5. In Shade, however, the Schmitt trigger is placed outside of the envelope detector and is used to convert the output of the envelope detector to a binary signal (i.e., logical 1 or 0) suitable for input to a computer or to event counter. *See* Column 5, lines 16-20. Therefore, the cited references do not specify all claim limitations and the use of an external Schmitt trigger in Shade to create a binary 0 and 1 output does not suggest adding a Schmitt trigger inside the envelope detector in order to smooth out the effect of signal glitches in the output voltage.

2. The Examiner Rejected the Claims by Relying on Impermissible Piecemeal, Hindsight Combination of References

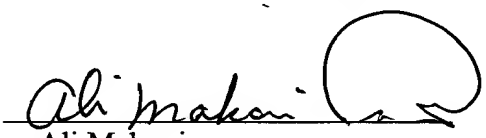
From the three cited references, neither Straver nor Kobayashi has any indication or suggestion of using a Schmitt trigger in an envelope detector. Shade, teaches away from including a Schmitt trigger in an envelope detector by applying the output of the envelope detector to a Schmitt trigger that is external to the envelope detector. *See* Shade Figure 1, items 29 and 37. Furthermore, in applying the output of the envelope detector to an external Schmitt trigger, Shade has the different motivation of converting the output of the envelope detector to a binary 0 or 1 as opposed to

motivation of the present invention to smooth out the effect of signal glitches in the output voltage. *See* Column 5, lines 16-20.

Therefore, Appellants respectfully submit that the cited references do not suggest the desirability of including a Schmitt trigger inside an envelope detector and the Examiner used impermissible piecemeal, hindsight combination of references in rejecting claims 8 and 11. In addition, Appellants respectfully submit that the Examiner, in making this rejection, did not identify any suggestion or motivation in the art for combining the two references without the identification of a suggestion or motivation to combine the cited references, the examiner has not met his prima facie case of obviousness.

CONCLUSION

In view of the foregoing, Appellants respectfully submit that the claims are patentable and the drawings fully comply with the appropriate rules. Appellants hereby request that the Board overturn the Examiner's finding that the claims are unpatentable under 35 U.S.C. 103(a).

BY: 

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CLAIMS APPENDIX

The following claims are the subject of this Appeal.

1. An envelope detector for determining whether the level of a differential input signal DPIN – DNIN is above a reference voltage V_{REF}, the envelope detector comprising:

(a) means for converting the differential input signal to a differential current IDP - IDN and the reference voltage to a reference current I_{REF};

(b) means for comparing the currents to determine if $|IDP - IDN|$ is greater than I_{REF}; and

(c) means for indicating a valid differential signal when $|IDP - IDN|$ is greater than I_{REF}.

2. The envelope detector of Claim 1, wherein the means for determining if $|IDP - IDN|$ is greater than I_{REF} includes a first comparator for comparing IDP - IDN with I_{REF} and a second comparator for comparing IDN - IDP with I_{REF}.

3. The envelope detector of Claim 2, wherein the means for indicating a valid differential signal includes an OR circuit coupled to the comparators for providing an output signal when IDP - IDN > I_{REF} or IDN - IDP > I_{REF}.

4. A method of determining whether the level of a differential input signal DPIN - DNIN

is above a reference voltage V_{REF}, the method comprising:

(a) converting the differential input signal to a differential current IDP - IDN;

(b) converting the reference voltage to a reference current I_{REF};

(c) comparing the currents to determine if $|IDP - IDN|$ is greater than I_{REF}; and

(d) indicating a valid differential signal when $|IDP - IDN|$ is greater than I_{REF}.

5. The method of Claim 4, wherein the currents are compared by comparing IDP - IDN and IDN - IDP with I_{REF}, and the valid differential signal is indicated if either IDP - IDN or IDN - IDP is greater than I_{REF}.

6. An envelope detector for determining whether the level of a differential input signal DPIN - DNIN is above a reference voltage V_{REF}, the differential input signal being cyclical with DPIN and DNIN each being greater than the other during alternate cycles and crossing over during a switching interval between the cycles, the envelope detector comprising:

(a) means for converting the differential input signal to a differential current IDP - IDN and the reference voltage to a reference current I_{REF};

(b) means for comparing the currents and providing an output signal indicative of a valid differential signal when $|IDP - IDN|$ is greater than I_{REF}; and

(c) means for maintaining the output signal during the switching interval following a cycle in which $|IDP - IDN|$ is greater than I_{REF}.

7. The envelope detector of Claim 6, wherein the means for comparing the currents includes a first comparator for comparing IDP - IDN with I_{REF} and a second comparator for comparing IDN - IDP with I_{REF}, and the means for providing the output signal includes an OR circuit coupled to the comparators for providing the output signal when IDP - IDN > I_{REF} or IDN - IDP > I_{REF}.

8. The envelope detector of Claim 7, wherein the means for maintaining the output signal comprises a Schmitt trigger responsive to the output signal from the OR circuit.

9. A method for determining whether the level of a differential input signal DPIN - DNIN is above a reference voltage V_{REF}, the differential input signal being cyclical with DPIN and DNIN each being greater than the other during alternate cycles and crossing over during a switching interval between the cycles, the method comprising:

(a) converting the differential input signal to a differential current IDP - IDN and the reference voltage to a reference current I_{REF};

(b) comparing the differential current and the reference current;

(c) providing an output signal indicative of a valid differential signal when $|IDP - IDN|$ is greater than I_{REF}; and

(d) maintaining the output signal during the switching interval following a cycle in which $|IDP - IDN|$ is greater than I_{REF}.

10. The method of claim 9, wherein IDP - IDN and IDN - IDP are compared with I_{REF}, and the output signal is provided when $IDP - IDN > I_{REF}$ or $IDN - IDP > I_{REF}$.

11. The method of claim 9, wherein the output signal is passed through a Schmitt trigger having trigger levels set further apart than a change in the output signal during the switching interval.

EVIDENCE APPENDIX

There is no evidence submitted by Appellants, the Appellants' legal representative, or assignees thereof.

RELATED PROCEEDINGS APPENDIX

There are no related appeals or interferences known to Appellants, the Appellants' legal representative, or assignees thereof.